

Atty. Docket No. OF03P212/US
Serial No: 10/733,884

Remarks

In the present Amendment, previously pending Claims 3 and 4 have been cancelled, and the subject matter formerly therein combined with Claim 1. Thus, no new matter is introduced by the present Amendment, and no new issues are believed to be raised by the present Amendment requiring further search or consideration beyond that already given to previous claims 1, 3 and 4.

The present invention relates to a semiconductor device and a method of manufacturing a semiconductor device having a plurality of via holes in each of a plurality of parts of an insulating layer. In each aspect of the invention, each of the plurality of via holes in a given insulating layer part exposes a (common) conductive line. In some aspects, each of the parts of the insulating layer (other than the via holes) has a certain thickness greater than zero but less than the insulating layer thickness (e.g., Claims 1 and 16), and/or trenches are etched in the insulating layer (e.g., Claims 1 and 10). In one aspect of the invention, each trench enables electrical connection of a subsequently formed conductive layer through a corresponding plurality of via holes to the exposed conductive line (e.g., Claim 10). However, claims 10-21 have been constructively withdrawn by the Examiner. Consequently, the following discussion will focus on claims 1 and 5-9.

The references cited against the present claims (Agarwala et al., U.S. Pat. No. 6,734,090 [hereinafter "Agarwala"], alone or together with Jahnes et al., U.S. Pat. No. 6,380,003 [hereinafter "Jahnes"]) neither disclose nor suggest etching parts of an insulating layer where a plurality of via holes will be formed to a certain thickness so as not to expose a first conductive line, selectively etching a plurality of via holes in each such part of the insulating layer, and etching trenches in the insulating layer, using three photoresist patterns as etching masks (see, e.g., Claim 1). At most, the references suggest only etching a plurality of via holes and etching trenches in the insulating layer to a certain thickness (a so-called "dual damascene" or "double damascene" process). Since the references disclose only the "via first" approach to the "double damascene" process, and neither reference discloses or suggests forming both trenches and a plurality of parts in which via holes will be formed, the references (alone or in combination) cannot disclose or suggest etching a plurality of via holes in each of a plurality of parts of the

Atty. Docket No. OF03P212/US
Serial No: 10/733,884

insulating layer that have been etched to a certain thickness so as not to expose a first conductive line. Consequently, the present claims are patentable over the cited references.

The Rejection of Claims 1, 3-7 and 9 under 35 U.S.C. § 102(e) is Respectfully Traversed

The rejection of Claims 1, 3-7 and 9 under 35 U.S.C. § 102(e) as being anticipated by Agarwala is respectfully traversed.

Agarwala discloses a method of making an edge seal for a semiconductor device (Title). Agarwala defines a via-stud pattern on (sacrificial dielectric) layer 18 by a photolithographic process, followed by sequential etching of layer 18, hard mask layer 16 and partially etching low-k dielectric 14 with suitable conventional etchants (col. 6, ll. 21-33 and FIG. 3B). The pattern for metal interconnection lines is next defined, again by a photolithographic process, followed by further etching of layer 18, hard mask 16, the remainder of low-k dielectric 14, and bottom dielectric layer 12 to form trenches 28 (for interconnection lines) and holes 26 (for via-studs) to expose metal line 24, initial process steps of the method conventionally known in the art as a double damascene method (col. 6, ll. 33-41 and FIG. 3B). In this process, at most two photoresist patterns are used as etching masks.

Applicant's undersigned representative does not necessarily agree with the interpretation of this passage from Agarwala given in the Office Action dated March 25, 2005 (sec, e.g., p. 7, paragraph a). It is not at all clear how a single step of partially etching via holes reads on a process that involves two separate etching steps (first, etching parts of an insulating layer where a plurality of via holes will be formed, and second, etching the plurality of via holes in each of the parts). Either Agarwala partially etches a plurality of via holes (in which case, there is no etching of the insulator layer parts where the plurality of via holes will be formed), or Agarwala partially etches parts of an insulator layer where, at most, a single via hole will be formed in each such part. However, this point may be moot in view of the present Amendment.

Agarwala discloses another embodiment, in which the edge seal is comprised of dual walls with one wall being metallic and the other wall being made of a dielectric material (col. 7,

Atty. Docket No. OF03P212/US
Serial No: 10/733,884

ll. 41-43). First, a photolithographic pattern is defined atop composite dielectric layers 12, 14, 16 (as described previously) followed by etching thereof to form a set of cavities 50 and 52 *and to expose metal line 24* (col. 7, ll. 44-49 and FIG. 4A; emphasis added). Subsequently, a set of cavities for via-studs 26 and for interconnection lines 28 are next formed in the low-k dielectric 14 using the methods of double damascene as described above (col. 7, ll. 59-62 and FIG. 4C).

Thus, Agarwala does not disclose or suggest etching parts of an insulating layer where a plurality of via holes will be formed to a certain thickness *so as not to expose a first conductive line*, selectively etching a plurality of via holes in each such part of the insulating layer, *and* etching trenches in the insulating layer. Consequently, Agarwala does not anticipate the present Claim 1.

Claims 5-7 and 9 depend from Claim 1, and thus include all of the limitations of Claim 1. (Claims 3 and 4 have been cancelled.) Therefore, Claims 5-7 and 9 are not anticipated by Agarwala for at least the same reasons as Claim 1. Consequently, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claim 8 under 35 U.S.C. § 103(a) is Respectfully Traversed

The rejection of Claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Agarwala in view of Jahnes is respectfully traversed.

As explained above, Agarwala does not disclose or suggest etching parts of an insulating layer where a plurality of via holes will be formed to a certain thickness *so as not to expose a first conductive line*, selectively etching a plurality of via holes in each such part of the insulating layer, *and* etching trenches in the insulating layer, as is recited in the present Claim 1. As will be explained below, Jahnes does not cure the deficiencies of Agarwala with regard to the present Claim 1. Consequently, this ground of rejection is also unsustainable, and should be withdrawn.

Jahnes discloses a substrate having a first level of electrically conductive features formed thereon; a patterned interlevel dielectric material formed on the substrate, wherein the patterned

Atty. Docket No. OF03P212/US
Serial No: 10/733,884

interlevel dielectric includes via spaces, and at least one of said via spaces is a slot via in which an anti-fuse material is formed on a portion thereof, and a second level of electrically conductive features formed in the spaces, whereby the anti-fuse material in the slot via provides a connection between the first and second levels of electrically conductive features (Abstract). FIG. 2c discloses via 58 and slot via 60 formed in interlevel dielectric 54, *to expose portions of the first level of electrically conductive features 52* (col. 4, ll. 21-29). Thus, to the extent via 58 and/or slot via 60 represent a part of an insulating layer where a plurality of via holes will be formed, they are not etched to a certain thickness *so as not to expose a first conductive line*.

Jahnes then teaches patterning a photoresist 64 to provide spaces 66 which correspond to positions in which the second level of electrically conductive features will subsequently be formed (col. 5, ll. 4-11; also see FIG. 2e). A portion of the patterned photoresist remains over the first level of electrically conductive features in the slot via (col. 5, ll. 11-14 and FIG. 2f). Thus, Jahnes discloses at most two photolithographic patterns for use as etching masks, similar to the "double damascene" process disclosed by Agarwala. Assuming this disclosure of Jahnes is analogous to conventional dual damascene processing, spaces 66 appear to correspond to trenches, in which case Jahnes does not disclose etching parts of an insulating layer where a plurality of via holes will be formed to a certain thickness *so as not to expose a first conductive line*. To the extent spaces 66 represent a part of an insulating layer where a via hole is formed, a plurality of via holes are not formed in each space (much less will be formed in each such space), and no trenches are subsequently formed.

By virtue of its silence with regard to (1) forming a plurality of via holes in a part of an insulating layer having a thickness greater than zero, but less than the insulating layer thickness, and (2) etching both trenches and parts of an insulating layer in which a plurality of via holes are formed, Jahnes is farther removed from the present Claim 1 than is Agarwala. The only structure in which Jahnes appears to form a plurality of via holes is the insulator layer 54 itself. Thus, Jahnes does not cure the deficiencies of Agarwala with respect to the method of Claim 1.

Atty. Docket No. OF03P212/US
Serial No: 10/733,884

Claim 8 depends from Claim 1, and thus includes all of the limitations of Claim 1. Therefore, Claim 8 is patentable over Agarwala in view of Jahnes for essentially the same reasons as Claim 1.

Conclusion

In view of the above amendments and remarks, the grounds of rejection are believed to be overcome, and the application is believed to be in condition for allowance. Furthermore, in view of the lack of reasonable and/or plausible basis for restriction between claims 1 and 3-9 (Group I) and claims 16-21 (Group II), and the complete lack of any basis at all for requiring an election of either claims 1 and 3-9 (Group A) and claims 10-15 (Group B), Applicant is entitled to further examination of claims 10-21. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



Andrew D. Fortney, Ph.D.
Reg. No. 34,600

7257 N. Maple Avenue, Bldg. D, #107
Fresno, California 93720
(559) 299 - 0128